

PRO DVX

THE ART OF DIGITAL VIEWING



INTEGRATED NFC

Technical Details

Basic Specification

Hardware Specification

Main Chip	NXP PN553
Frequency	13.56MHz
Host Interface	NCI Protocol Interface according to NFC Forum NCI 1.0 standardization I2C High-Speed mode supported
Connector	15 pin FPC/FFC
NFC Standard	<ul style="list-style-type: none">● ISO/IEC 14443 A● ISO/IEC 14443 B● ISO/IEC 15693● MIFARE 1K/4K● MIFARE DESFire● Sony Felica
Operation Temperature	-10~75 degrees Celsius

Hardware Pin Define

HOST Pin define

Pin number	Name	Configuration	Description
1	VBAT	Power Supply Input	Module Power Supply
2	GND	Power Supply Ground	Module Ground
3	SWP_UICC	Input / Output	Single Wire Protocol line to UICC / SIM
4	NA	NA	No Function (unused pin)
5	IRQ	Output	Interrupt request from module to platform
6	VDD_SIM (PMUVCC)	Power Supply Input	The power rail used to power UICC / SIM
7	I2C_SDA	Input / Output	I2C data
8	I2C_SCL	Input	I2C clock
9	GND	Input	Module Ground
10	Reset / Wake Up	Input	Reset pin input from the host to wake up the device from standby and also to reset the device
11	DWL_REQ	Input	Control pin to set the NFC Module in firmware download mode
12	SWP_PWR (SIM_VCC)	Power Supply Output	Power supply to UICC / SIM or power supply 'request' to PMIC
13	VBAT	Power Supply Input	Module Power Supply
14	VDD_IO	Power Supply Input	Host IO reference voltage
15	GND	Power Supply Ground	Module Ground

System Architecture

